

Certess' Certitude Extends Functional Qualification to Include Designs Created in SystemVerilog

Certitude supports Cadence Incisive (NC-Sim), Mentor Graphics ModelSim® and Synopsys VCS®-MX

CAMPBELL, Calif. – May 14, 2008 – Certess, Inc., the provider of functional qualification tools for systems on a chip (SoCs) and intellectual property (IP) blocks, today announced that Certitude now qualifies designs created in SystemVerilog, including mixed language designs with Verilog and VHDL. Certitude supports the three most common simulators in integrated circuit (IC) design: Cadence Incisive (NC-Sim), Mentor Graphics ModelSim® and Synopsys VCS®-MX.

Certitude, the first commercial functional qualification software tools for companies developing IP blocks or integrating SoCs, qualifies the whole verification process and removes the uncertainty that accompanies many design projects. SystemVerilog, the industry's first unified hardware description and verification language standard, has been adopted by hundreds of semiconductor design companies and is supported by more than 75 electronic design automation (EDA), IP (intellectual property) and training solutions worldwide. Adding support for SystemVerilog to Certitude helps designers improve productivity in the design and verification of large gate-count, IP-based chips.

Certitude addresses two of the most critical problems associated with the design of semiconductors: first, that the functional verification process consumes more resources than the design process; and second, despite having a set of dedicated tools and methodologies that automate parts of the process and improve verification quality, companies find that functional logic errors are still the largest cause of silicon respins. Certitude certifies that if a semiconductor chip design had a bug, it would be found.

Certitude pricing starts at US \$100,000 per year.

About Certess

Certess, Inc. is the only electronic design automation company providing functional qualification products for companies that create and integrate complex design blocks or intellectual property (IP). The company's technology provides design and verification engineers with an objective way to evaluate and improve the completeness of the verification environment, resulting in a shorter and more predictable process to integrate SoC designs and ensure high quality designs. The company is headquartered in Campbell, CA. For additional information, see www.certess.com.

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